



Agilent Technologies 10010982
Apparatus For Routing Electrical Signals
Inventor(s): William S Burton

Replacement Sheet

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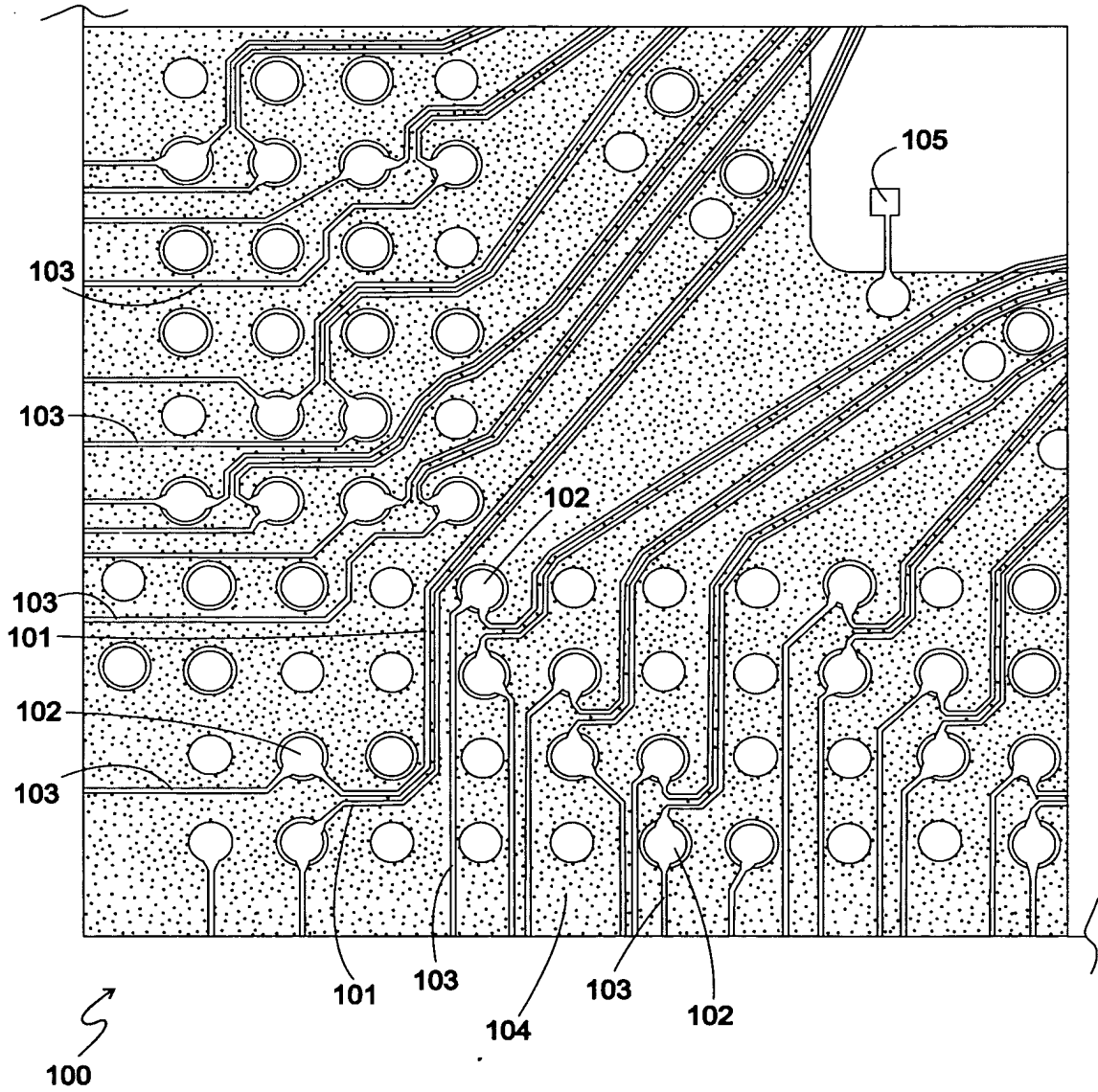


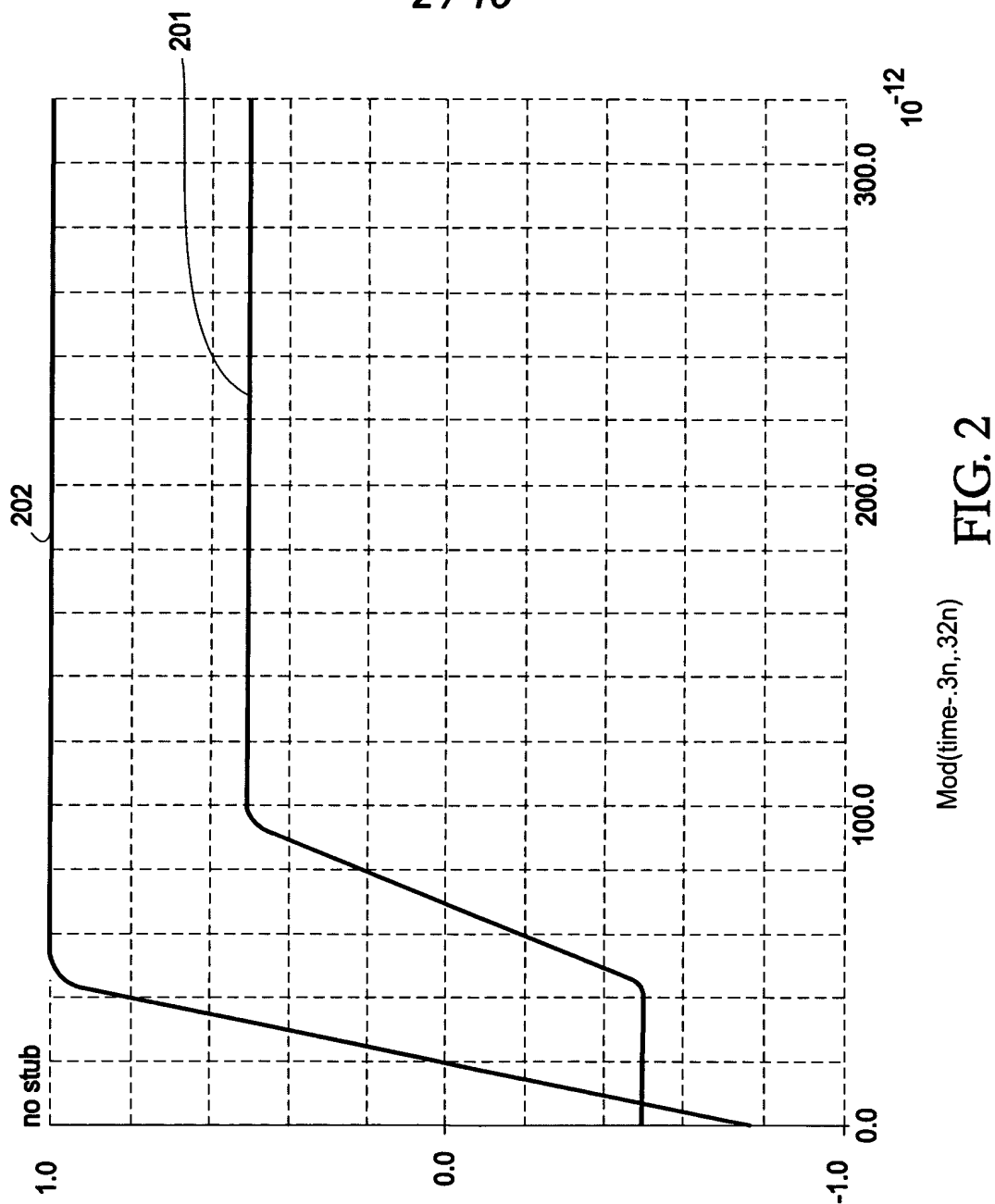
FIG. 1 Prior Art

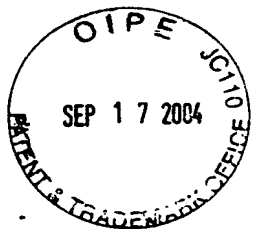


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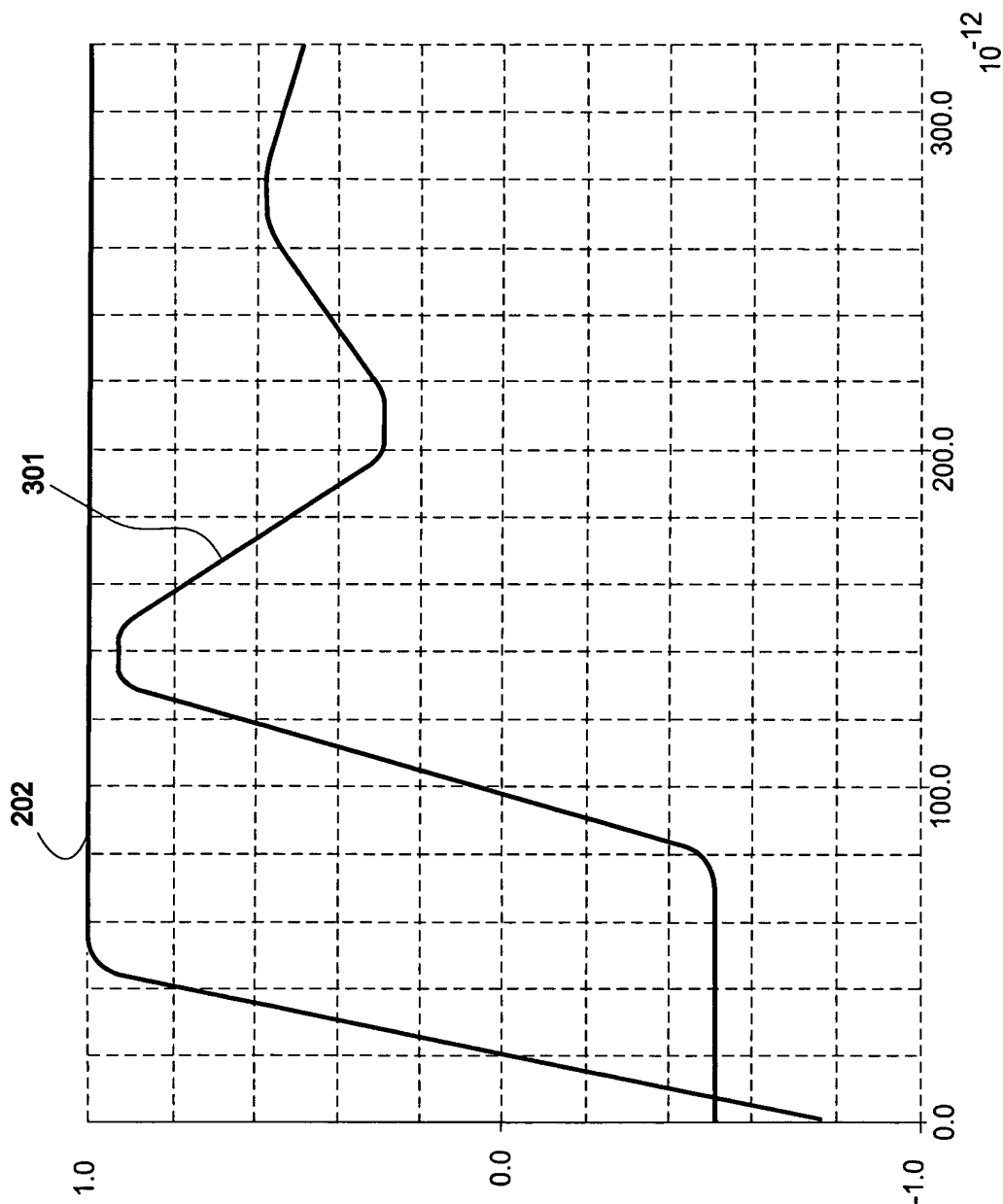




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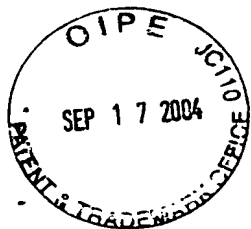
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Mod(time-.3n,.32n)

FIG. 3



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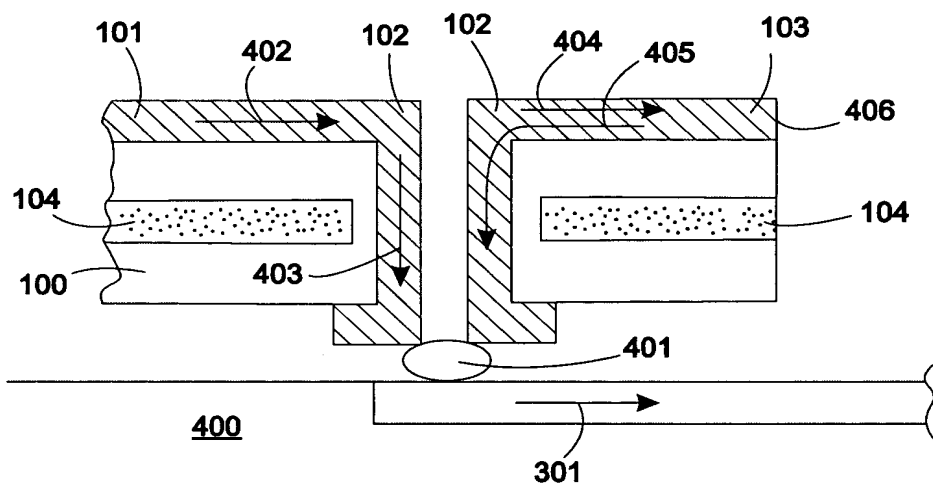
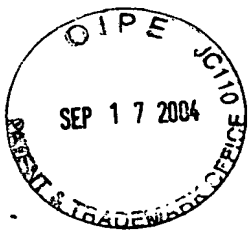


FIG. 4



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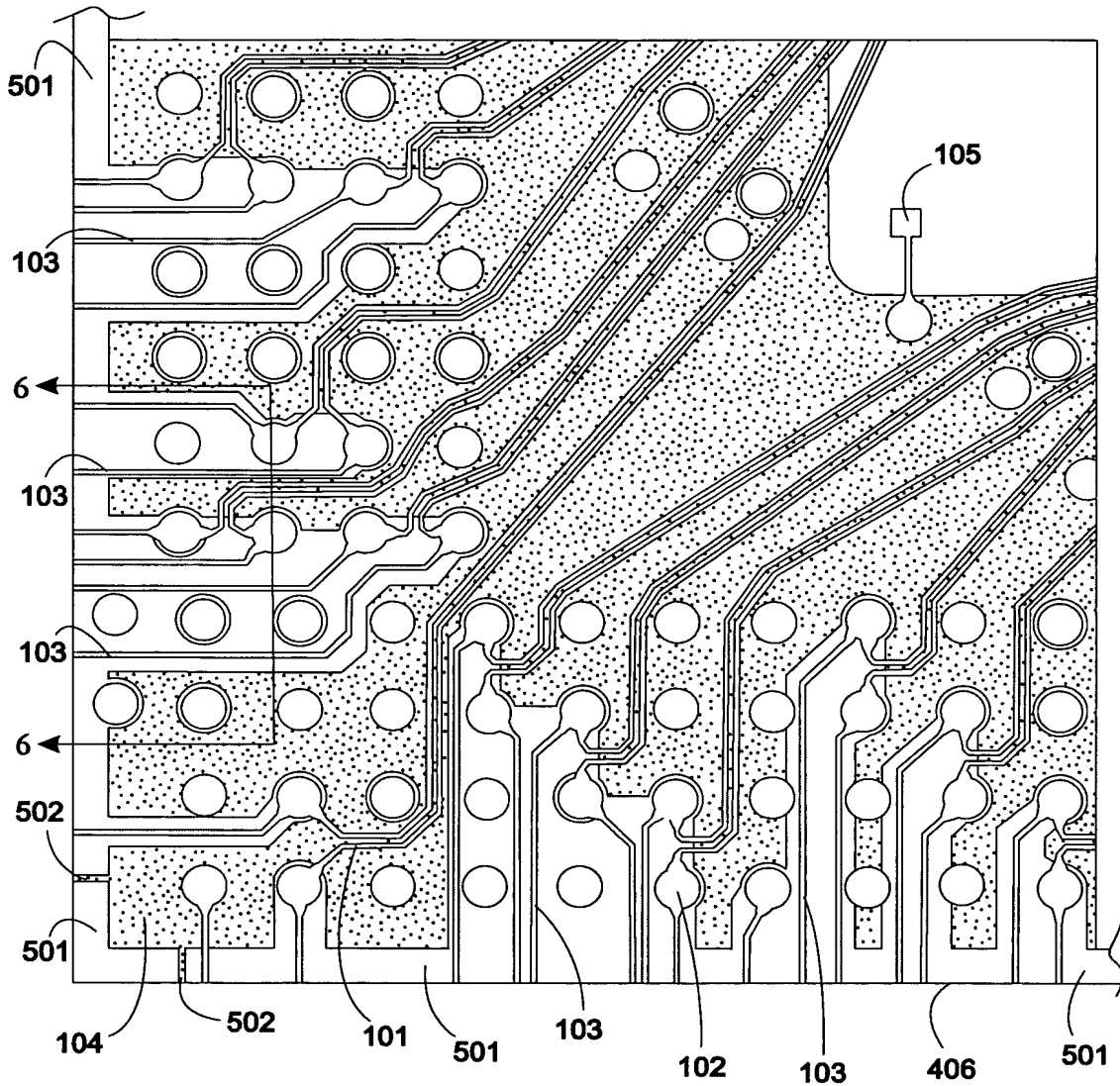
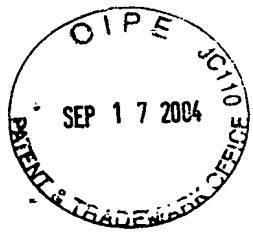


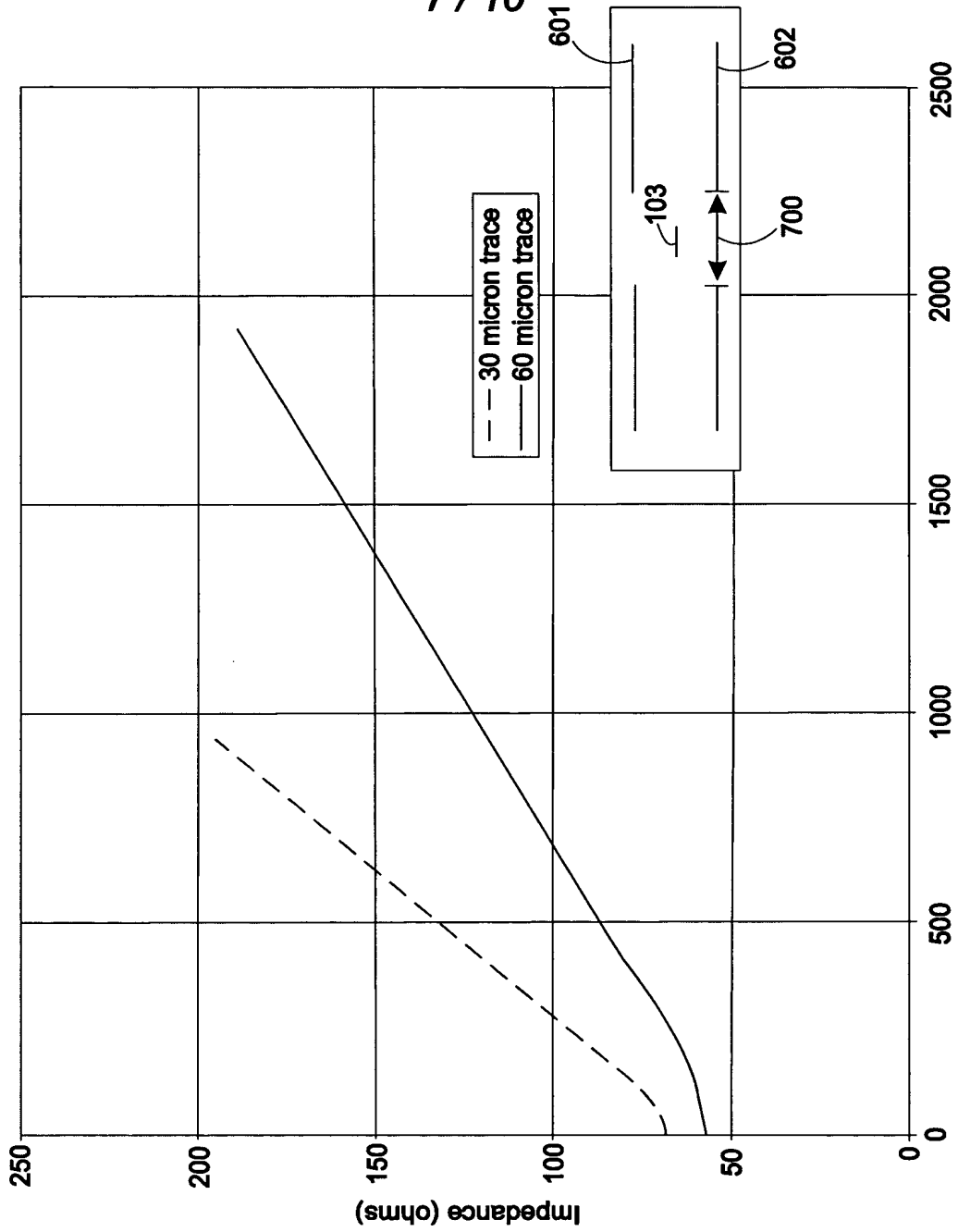
FIG. 5

Figure 1 consists of three cross-sectional diagrams labeled (a), (b), and (c), illustrating the manufacturing process of a semiconductor device. In diagram (a), a substrate 102 is shown with a first layer 601 and a second layer 602. A third layer 103 is formed on top of the first layer 601. In diagram (b), the third layer 103 is being etched away from the first layer 601, leaving it on the second layer 602. In diagram (c), the final structure is shown with the first layer 601 and second layer 602, and the third layer 103 removed.



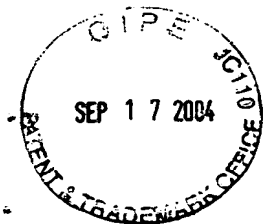
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Gap width above and below trace (microns)

FIG. 7



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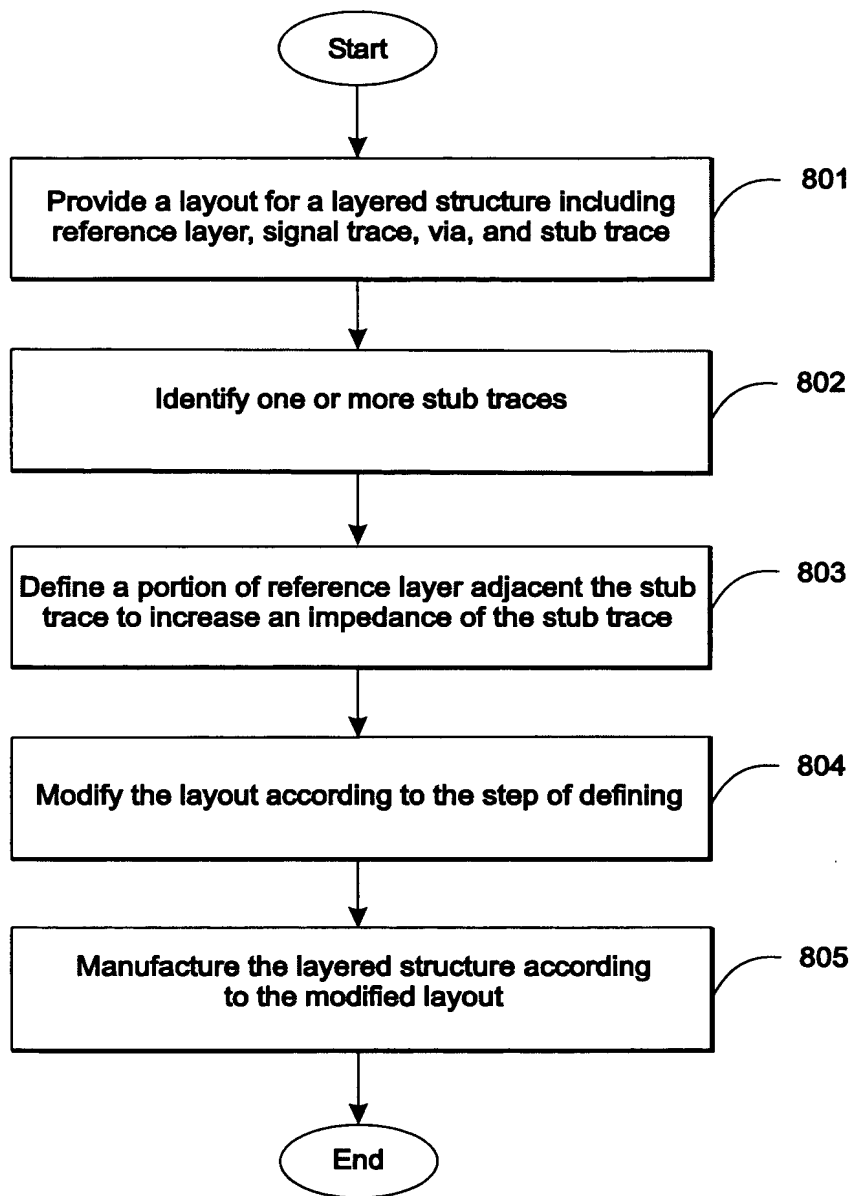
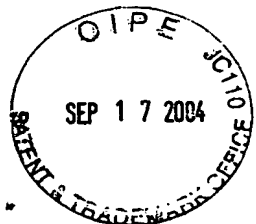


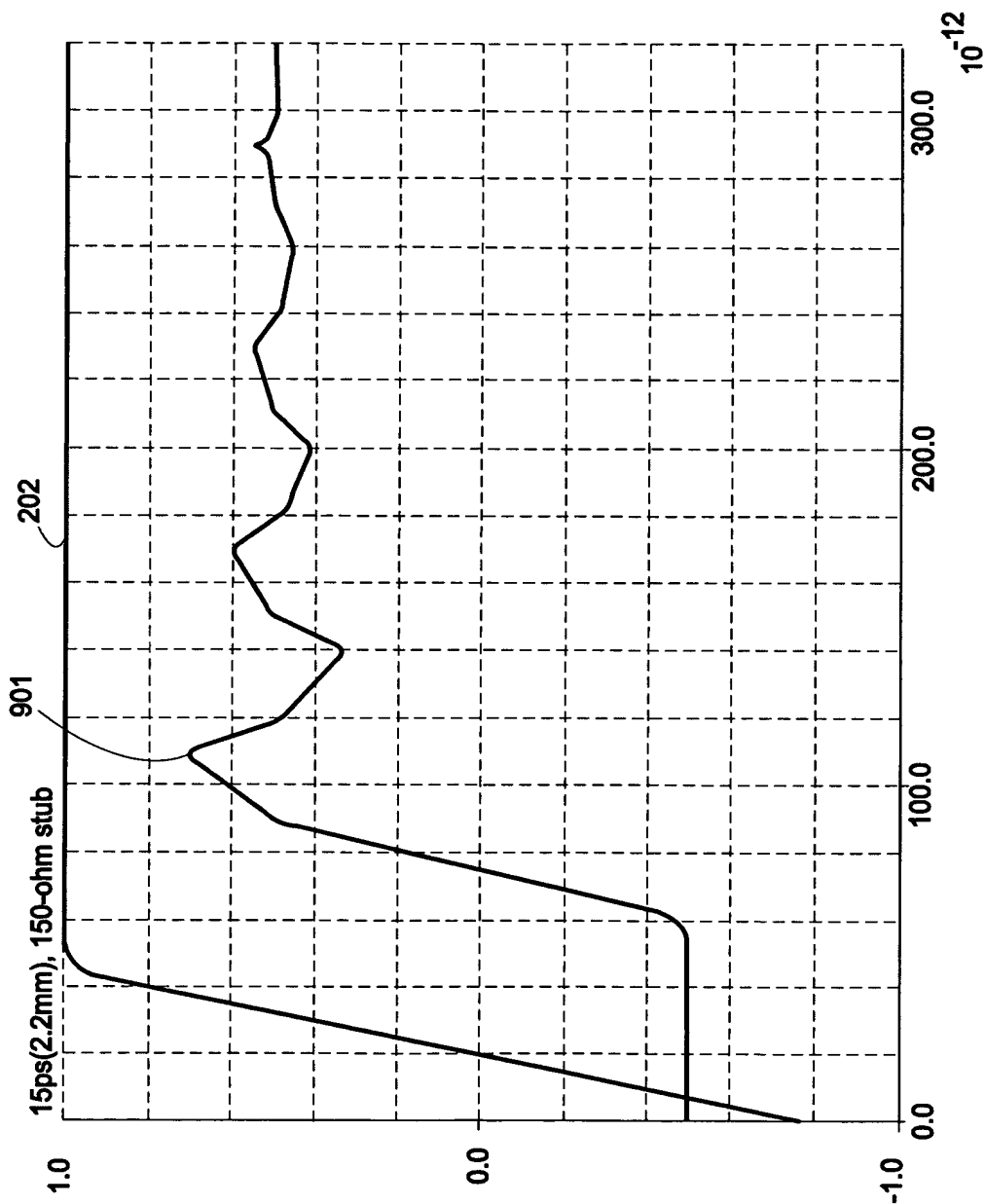
FIG. 8



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Mod(time-.3n,.32n)

FIG. 9



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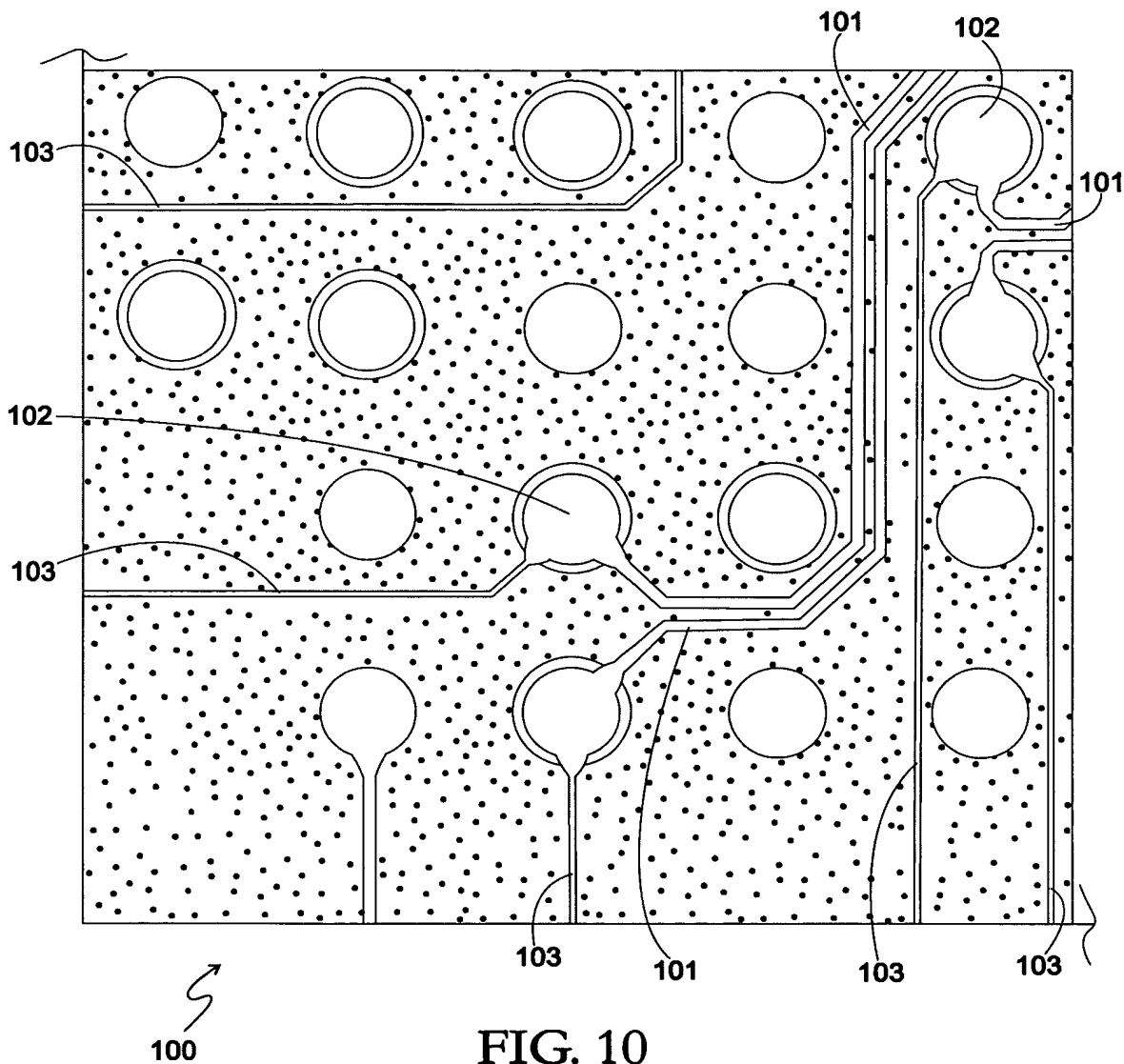


FIG. 10